REMARKS

Claims 1 and 3-15 are pending in the present application. Figures 1-4 and claim 1 have been and claim 2 canceled amended by way of the present amendment. Reconsideration is respectfully requested.

In the outstanding Office Action, Figures 1-3 have been indicated as needing a legend, such as Prior Art; claims 1-6 and 13-15 were rejected under 35 U.S.C. Section 103(a) as unpatentable over the Applicant's Prior Art Figure 2B (APAF) in view of U.S. Patent Publication No. 2002/0122280 (Ker et al. I); claims 7, 8 and 10-12 were rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of U.S. Patent No. 6,566,715 (Ker et al. II); and claim 9 was rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of Ker et al. II as applied to claim 7 above, and further in view of Ker et al. I.

Drawing Objections

Figures 1-3 were indicated to need a legend such as Prior Art. In response to the rejection, Figures 1-3 have been amended to include the legend "Background Art." Replacement sheets for Figures 1-3 including the legend "Background Art" are filed herewith. In addition, FIG. 4 has been amended to correct a drawing error. In particular, Patent Application Publication No. US 2005/0224882 A1 discloses at page 3, paragraph [0027], lines 6-7 states: "N-well **38** and N-well **37** are connected through contact **36**, **30** to VDD." FIG. 4 has been amended to correctly illustrate this concept from the disclosure. Thus, Applicants respectfully submit that the amendments raise no question of new matter. As a result, Applicants request that the outstanding drawing objection be withdrawn.

35 USC Section 103 Rejections

Claims 1-6 and 13-15 were rejected under 35 U.S.C. Section 103(a) as unpatentable over APAF in view of Ker et al. I. Applicants respectfully traverse the rejection.

It is noted that claim 2 recites: "wherein said substrate has a contact which is outside of said first, second and third wells." In order clarify the invention, this limitation has been incorporated into claim 1. Claim 7 as originally presented reads similarly in reciting: "a substrate contact located outside of said wells." Claim 13, as previously presented included this limitation in reciting: "substrate contacts located outside of said first, second and third wells." Support for the limitation is provided at least at page 3, paragraph [0027], lines 11-12; and shown at least in FIG. 4, references **44, 50** of the published application.

The APAF discloses the implementation of an ESD NMOSFET in a triple well CMOS architecture.[1] In particular, the APAF discloses an additional N-Band **40** that constitutes an n-type doped region which in combination with the N-Wells **37** and **38** isolates the P-well **31** from the substrate **41**.[2] As can be seen from FIG. 2B of the specification, the triple well architecture of the background art is similar to the dual well architecture, *with the exception of the additional N-Band **40**, and N-wells **37** and **38***.[3] N-wells **37** and **38** are connected in the embodiment shown to a source of positive potential VDD.[4] Additionally, two isolation regions **33** and **34** provide isolation for N-well **37** and N-well **38** from the substrate contact **30** and drain **26**, respectively.[5]

However, the APAF nowhere discloses, as recited in independent claim 1:

> *a path of substrate material extending through an opening in said conductive band region*, increasing the substrate resistance in the path of the current which flows through said I/O pad to a

[1] *Id.* at page 2, paragraph [0024], lines 1-2.
[2] *Id.* at page 2, paragraph [0024], lines 2-5.
[3] *Id.* at page 2, paragraph [0024], lines 5-8.
[4] *Id.* at page 2, paragraph [0024], lines 8-10.
[5] *Id.* at page 2, paragraph [0024], lines 10-12.

> substrate contact and drain during an ESD event and electrically connecting the second well to the substrate,
>
> wherein *said substrate* has a contact which is outside of said *first, second and third wells* (emphasis added).

That is, the APAF nowhere discloses: "the substrate contact is located outside the first, second and third wells;" as recited in the presently amended claim 1 and as was originally cited in claim 13. Therefore, the APAF does not disclose the claimed invention.

In addition, the outstanding Office Action acknowledges deficiencies in the APAF and attempts to overcome these deficiencies by combining the APAF with Ker et al. I. However, Ker et al. I cannot overcome all of the deficiencies of the APAF as will be discussed below.

Ker et al. I discloses an electrostatic discharge (ESD) protection component with a deep-N-well structure in CMOS technology.[6] In particular, Ker et al. I discloses an N-type Silicon Controlled Rectifier (NSCR) device with a deep N-well, as shown in FIG. 5. Further, Ker et al. I discloses that there are three nodes in the NSCR structure: (1) the anode; (2) the cathode; and (3) the control gate (VGN).[7]

In addition, Ker et al. I discloses that the PNPN structure of the NSCR is composed of the P+ diffusion **52**, the N-well **42**, the P-well **40** and the N+ diffusion **46**.[8] The P+ diffusion **52** is used as the anode of the NSCR device and an NMOS is inserted into the P-well **40**.[9] The drain of the NMOS is formed by the N+ diffusion **44** at the P-N junction of the P-well **40** and the N-well **42**.[10] The source of the NMOS is formed by the N+diffusion **46**, used as the cathode of the NMOS device.[11]

---

[6] Ker et al. I at ABSTRACT.
[7] *Id.* at page 3, paragraph [0047], lines 2-4.
[8] *Id.* at page 3, paragraph [0047], lines 4-6.
[9] *Id.* at page 3, paragraph [0047], lines 6-8.
[10] *Id.* at page 3, paragraph [0047], lines 8-10.
[11] *Id.* at page 3, paragraph [0047], lines 10-11.

Further, Ker et al. I discloses that in this modified device structure, the P-well **40** of the NSCR device is partially connected to the common P-substrate **30**.[12] But the two deep N-well regions **3201** and **3202** are placed closer to limit the connection region of the P-well **40** and the P-substrate **30**, thereby increasing the equivalent resistance between them.[13] The deep N-well **3201** is connected to N-well **60**, the deep N-well **3202** is connected to N-well **42**.[14] When proper voltage is applied to the control gate VGN, the trigger current from the NMOS into the P-well **40** turns on the NSCR more quickly within the limited connection region.[15] Moreover, Ker et al. I discloses that the P-substrate **30** is connected to VSS *through the P-well* **36** and the P+ diffusion **54** (emphasis added).[16]

However, it is respectfully submitted that Ker et al. I cannot overcome all of the deficiencies of the APAF regarding claim 1 and in particular regarding claim 5. As discussed above, the APAF discloses a substrate contact **30** within a well **37**. Though Ker et al. I discloses a structure for improving ESD performance that includes a substrate contact **54** outside of wells **40**, **42** and **60**, it is respectfully submitted that the structure/function of Ker et al. I is so different from the APAF that attempting to make this combination would destroy the intended ESD purpose of the structure of the APAF. In addition, it is noted that there is nothing in either of the references that would suggest it is known outside of the application to combine the references to obtain applicants particular structure.

Regarding claim 5, the combination of the APAF and Ker et al. I does not disclose both "a substrate contact located outside of first, second and third wells" and a "gate connection and source connected to said substrate contact." That is, the gate connection and source connected to said substrate of the APAF is inside a well. It is respectfully submitted that modifying the APAF as in Ker et al. I would destroy the intended function of the APAF.

[12] *Id.* at page 3, paragraph [0047], lines 11-13.
[13] *Id.* at page 3, paragraph [0047], lines 14-17.
[14] *Id.* at page 3, paragraph [0047], lines 17-18.
[15] *Id.* at page 3, paragraph [0047], lines 14-21.
[16] *Id.* at page 3, paragraph [0044], lines 19-20.

In addition, it is noted that Ker et al. I discloses a substrate contact **54** that is connected to VSS.[17] In contrast, the claimed invention discloses a substrate contact **50** connected to VDD. That is, Ker et al. I teaches away from the disclosed structure and function of the APAF. That is, as discussed above, the APAF clearly does not include an opening in the N-Band **40**. Further, Ker et al. I nowhere discloses the structure recited in claim 1 of: "first, second and third wells formed in the substrate and separated by shallow well isolation regions."

The arguments made above for claims 1 are also applicable to claim 13 which recites: "substrate contacts located outside of first, second and third wells." The arguments made above with regard to claim 5 are also applicable to claim 14 which recites: "source and gate are connected to said substrate contact." Thus, at least for the reasons discussed above, claims 13 and 14 are not disclosed by the APAF and Ker et al. I.

Therefore, at least for the reasons above, it is respectfully submitted that neither the APAF nor Ker et al. I, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention and that claims 1, 5, 13 and 14, and claims dependent thereon, patentably distinguish thereover.

Claims 7, 8 and 10-12 were rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of Ker et al. II. Applicants respectfully traverse the rejection.

Claim 7 includes similar language to that found in claim 1. That is, claim 7, recites: "a substrate contact located outside of wells." Thus, at least for the reasons discussed above for claim 1, the APAF also does not disclose all of the limitations of claim 7.

The outstanding Office Action acknowledges deficiencies in the APAF and attempts to cure those deficiencies with Ker et al. II. However, Ker et al. II cannot overcome all of the deficiencies of the APAF as discussed below.

[17] Ker et al. I at FIG. 4b.

Ker et al. II discloses a substrate-triggered technique to effectively improve the ESD robustness of integrated circuit (IC) products.[18] In particular, Ker et al. II discloses a substrate-triggered NMOS is positioned in a p-well **32** on a p-substrate **30**.[19] Two poly-silicon gates **34**, serving as the gate (electrode) of the substrate-triggered NMOS, are positioned above the p-well **32**.[20] Two n+ doped regions **36**, functioning as the drain (electrode) of the substrate-triggered NMOS, are positioned between poly-silicon gates **34** on the surface of the p-well **32**.[21] Between the n+ doped regions **36**, a p+ doped region **40** is positioned for the electrical connection to p-well **32** and serves as the trigger node for the substrate-triggered NMOS.[22] Isolation object(s) **42**, in this example, the silicon oxide formed by the shallow trench isolation processes, isolate the p+ doped region **40** from the n+ doped regions **36**.[23] The two n+ doped regions **38** on the surface(s) of p-well(s) 32 provide the source (electrode) of the substrate-triggered NMOS.[24] As shown in FIG. 5B, one of the n+ doped regions **38**, a p-well **32** and one of the n+ doped region 36 together can construct a parasitic npn bipolar junction transistor (BJT).[25]

In addition, Ker et al. II discloses an n-well **44** is positioned to partially overlay and electrically couple with the n+ doped region **38**.[26] Beside the n+ doped region **38**, a p+ doped region **46** forms the electrical connection to p-well **32'**.[27] All the surfaces of the p+ regions **46** and **40** are capped by silicide material.[28] The areas of the n+ doped regions **36** and **38** are patterned by a photo mask **52** to block silicide material on their surfaces but the contact areas will be still covered with silicide.[29]

---

[18] Ker et al. II at ABSTRACT.
[19] *Id.* at column 1, lines 16-17.
[20] *Id.* at column 1, lines 17-20.
[21] *Id.* at column 1, lines 20-23.
[22] *Id.* at column 1, lines 23-25.
[23] *Id.* at column 1, lines 26-28.
[24] *Id.* at column 1, lines 28-31.
[25] *Id.* at column 1, lines 31-34.
[26] *Id.* at column 1, lines 35-36.
[27] *Id.* at column 1, lines 36-37.
[28] *Id.* at column 1, lines 37-39.
[29] *Id.* at column 1, lines 39-42.

Further, Ker et al. II discloses the contacts **54** for the n+ doped regions **36** must be separated from poly-silicon gate **34** by a specific distance, as shown in FIG. 5A, to sustain a higher ESD stress.[30] The shortest conductive path from the base of the npn BJT to the p+ doped region **46** must travel around n-well **44**, to take advantage of the higher resistance provided by spread resistor Rsub.[31]

However, it is respectfully submitted that Ker et al. II cannot overcome all of the deficiencies of the APAF regarding claim 7. In particular,

As discussed above, the APAF discloses a substrate contact **30** within a well **37**. Though Ker et al. II discloses a substrate contact **46** outside of wells **32** and **44**, it is respectfully submitted that the structure/function of Ker et al. II is so different from the APAF that attempting to make this combination destroys the intended purpose of the APAF. In addition, it is noted that there is nothing in either of the references that would suggest it is known outside of the application to combine the references to obtain the exact structure of applicants invention.

Further, it is respectfully submitted that Ker et al. II teaches away from the claimed invention. In particular, Ker et al. II discloses "an n-well is positioned to partially overlay and electrically couple with the n+ doped region **38**" and that "n+ doped regions 38 on the surface(s) of p-well(s) 32 provide the source (electrode)."[32]

Therefore, at least for the reasons above, it is respectfully submitted that neither the APAF nor Ker et al. II, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention and that claim 7, and claims dependent thereon, patentably distinguish thereover.

[30] *Id.* at column 1, lines 43-45.
[31] *Id.* at column 1, lines 45-49.
[32] *See Ker et al. II* at column 4, lines 30-33 and 35-38.

Claim 9 was rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of Ker et al. II as applied to claim 7 above, and further in view of Ker et al. I. Applicants respectfully traverse the rejection.

Claim 9 is dependent on claim 7. Thus, at least for the reasons discussed above for claim 7, the APAF and Ker et al. II do not disclose all of the limitations of claim 9. In addition, the outstanding Office Action acknowledges deficiencies in the APAF and Ker et al. II and attempts to cure those deficiencies with Ker et al. I. However, Ker et al. I cannot overcome all of the deficiencies of the APAF and Ker et al. II, as discussed below.

As discussed above, the APAF discloses a substrate contact **30** within a well **37**. Though Ker et al. I discloses a structure for improving ESD performance that includes a substrate contact **54** outside of wells **40**, **42** and **60**, it is respectfully submitted that the structure/function of Ker et al. I is so different from the APAF that attempting to make this combination would destroy the intended ESD purpose of the structure of the APAF. In addition, it is noted that there is nothing in either of the references that would suggest it is known outside of the application to combine the references to obtain applicants particular structure.

Therefore, at least for the reasons above, it is respectfully submitted that none of the APAF, Ker et al. I, and Ker et al. II, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention, and that claim 9, and claims dependent thereon patentably distinguish thereover.

Conclusion

Based on the above amendments and arguments, Applicant respectfully submits that the application is in condition for allowance. If a fee is due, please charge Deposit Account No. 50-3223, under Order No. 21806-00158-US, from which the undersigned is authorized to draw.

Dated: October 16, 2006
488146_1

Respectfully submitted,

By__/Myron K. Wyche/_____
Myron K. Wyche, Reg. No. 47,341
CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Agent for Applicant